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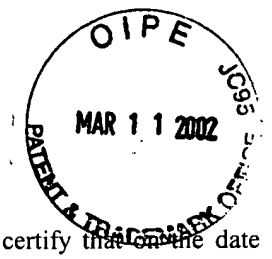


PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Box Non-Fee Amendment, Commissioner of Patents, Washington, DC 20231.

February 25, 2002 — Ayesha S. Wilks

Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Thomas W. Voshell	Attorney Docket No.:	500080.02
Serial No.	: 09/695,756	Group Art Unit	: 2133
Filed	: October 24, 2000	Examiner	: Samuel K. Lin
Title	: METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION		

Box Non-Fee Amendment
Commissioner of Patents
Washington, DC 20231

RESPONSE TO OFFICE ACTION

Sir:

Claims 41-67 are pending in the present application. In the office action mailed January 16, 2002, claims 49-53 were allowed and claims 44 and 65-67 were objected to as depending from a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims.

Claims 41 and 45 have been rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 5,363,382 to Tsukakoshi ("the Tsukakoshi patent"). Claims 42, 43, 46-48, and 54-64 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent alone, or in view of U.S. Patent No. 5,881,221 to Hoang *et al.* ("the Hoang patent").

Embodiments of the present invention are directed to a technique and system where memory locations in a spare memory can be substituted for defective memory in a system memory. As a result, a memory array may be operated more efficiently by reducing the number of memory cells needed in order to store a map of defective memory cells in the memory array. In operation, the addresses for the defective locations in the system memory are stored in a

compressed format in a map memory array. A range of these compressed defective addresses are stored in an uncompressed format in a temporary array. When a requested memory address is presented to a storage control unit, a hash code for the requested memory address is compared to hash codes for the uncompressed defective address currently stored in the temporary memory. In the event the hash code of the requested address matches one of the hash codes of the uncompressed defective addresses, then the address of the substitute memory location in a spare memory array corresponding to the matching hash code is provided by the temporary memory. The location in the spare memory is then accessed. However, in the event that the hash code does not match any of the hash codes for the uncompressed defective address currently stored in the temporary memory, compressed defective address information in the range of the hash code of the requested address is found in the map memory, decompressed, and then stored in the temporary memory. Then the hash code of the requested data is compared with the newly decompressed data. If there is a hash code match, then the substitute address is provided by the temporary memory. If there is not a hash code match, the storage control unit assumes that the requested memory address is not for a defective memory location, and proceeds to access the system memory.

In contrast, the Tsukakoshi patent describes a method of memory fault analysis for redundancy memory repair using a fault analysis memory (FAM) that is smaller than the memory area of the memory under test (MUT). This is accomplished by taking advantage of the particular redundancy arrangement of the MUT. The example described in the Tsukakoshi patent describes a MUT having a redundancy memory repair arrangement where redundant rows and columns of memory are replaced in pairs. That is, although only one row of memory cells may be defective, two rows of redundant memory are nevertheless substituted to repair the defective memory cells. Similarly, column redundancy are also substituted for defective memory cells in pairs. Thus, the method described in the Tsukakoshi patent takes advantage of this fact by having one memory location in the FAM correspond to four memory locations (arranged in a 2-by-2 square) in the MUT. That is, if any of the four memory cells are defective, then the corresponding single memory location stores a flag indicating that there is a defective cell.

Where the number of redundant memory rows are columns substituted for defective memory locations in the MUT are greater than two, the "compression" ratio of the method described by the Tsukakoshi patent would be increased. For example, if four redundant rows and columns are used when a replacement is made, then one memory location in the FAM could correspond to sixteen memory locations (arranged in a 4-by-4 square) in the MUT. Consequently, where any one of those sixteen memory cells of the MUT are defective, the single memory location in the FAM corresponding to those sixteen cells will store a flag indicating a defect.

Claims 41 and 45 are clearly patentably distinct from the teachings of the Tsukakoshi patent. Claim 41 recites a method for accessing a memory, comprising comparing a memory address of a memory access request to defective memory addresses stored in a compressed format, the defective memory addresses having substitute addresses associated and stored therewith, where the memory address matches one of the stored defective memory addresses, extracting the substitute address associated therewith, and accessing a memory location corresponding to the extracted substitute address rather than a memory location corresponding to the memory address. Claim 45 recites a method for accessing a memory device receiving memory addresses, the method comprising comparing the received memory addresses to addresses of defective memory locations in the memory device, the addresses of the defective memory locations having associated therewith substitute addresses corresponding to substitute memory locations in another memory, and substituting for the memory addresses matching the addresses of defective memory locations the associated substitute memory addresses to access the substitute memory locations in the other memory.

The examiner has failed to show how the Tsukakoshi patent describes the combination of elements recited in claims 41 and 45. With respect to the rejection of claim 41, the Examiner simply states that, "Tsukakoshi teaches memory fault analysis (access/test) by performing substitute address allocation (mapping) and compression [column 2, lines 35-50] as claimed." *See* office action, p. 2. The same rationale is used by the Examiner to support the rejection of claim 45. *Id.* It is well established that in order for an Examiner to establish a *prima facie* case of anticipates, the Examiner must be able to show that a reference teaches every element of a claim. *See* MPEP, section 2131. As previously discussed, the Examiner has failed

to establish a *prima facie* case of anticipation based on the Tsukakoshi patent because the Examiner has not shown where or how the Tsukakoshi patent teaches each element of claims 41 and 45.

Moreover, the teachings of the Tsukakoshi patent have little relevance to the subject matter of the present claims. Claim 41 and 45 recite combinations of limitations that can not be found anywhere in the Tsukakoshi patent. For example, as previously discussed, claim 41 recites comparing a memory address of a memory request to defective memory addresses stored in a compressed format, and where the memory address matches one of the stored defective memory addresses, extracting the substitute address associated therewith. The memory location corresponding to the substitute address is then accessed rather than the memory location corresponding to the address of the memory request. The Tsukakoshi patent does not teach any of these elements.

Consequently, the rejection of claims 41 and 45 under 35 U.S.C. 102(a) as being anticipated by the Tsukakoshi patent cannot be maintained. Therefore, the rejection of claims 41 and 45 should be withdrawn.

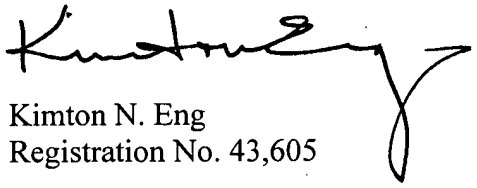
With respect to the rejection of claims 42, 43, 46-48, and 54-64 under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent, alone and in combination with the Hoang patent, the Examiner has also failed to establish a *prima facie* case of obviousness. It is also well known that in order to establish a prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *See* MPEP, section 2143.03. However, the Examiner has merely cited the Tsukakoshi patent as the basis of maintaining the rejection of these claims without identifying where in and how the Tsukakoshi patent would render the combination of elements recited in the claims unpatentable in view of what the Examiner contends to be obvious to one of ordinary skill in the art. As previously discussed, the Tsukakoshi patent fails to describe any of the elements of the claims alone or in combination with one another. Thus, even if we assume that the subject matter purported by the Examiner to be obvious is indeed obvious, this would still fail to make up for the deficiencies of the Tsukakoshi patent. The teachings of the Hoang patent also fail to make up for any of the deficiencies previously discussed. Moreover, many of the claims rejected as being unpatentable are patentable based on their dependency from allowable base claims.

For the foregoing reasons, claims 42, 43, 46-48, and 54-64 are patentable over the Tsukakoshi patent, alone or in combination with the Hoang patent or the subject matter found to be obvious by the Examiner. Therefore, the rejection of claims 42, 43, 46-48, and 54-64 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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